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APPLICATION FOR LETTERS PATENT

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Method And Apparatus For Testing Semiconductor Circuitry For Operability And Method Of Forming Apparatus For Testing Semiconductor Circuitry For Operability

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ATTORNEY'S DOCKET NO. MI28-027

TECHNICAL FIELD

This invention relates to methods for testing semiconductor circuitry for operability, and to constructions and methods of forming testing apparatus for operability testing of semiconductor circuitry.

BACKGROUND OF THE INVENTION

This invention grew out of the needs and problems associated with multi-chip modules, although the invention will be applicable in other technologies associated with circuit testing and testing apparatus construction. Considerable advancement has occurred in the last fifty years in electronic development and packaging. Integrated circuit density has and continues to increase at a significant rate. However by the 1980's, the increase in density in integrated circuitry was not being matched with a corresponding increase in density of the interconnecting circuitry external of circuitry formed within a chip. Many new packaging technologies have emerged, including that of "multichip module" technology.

In many cases, multichip modules can be fabricated faster and more cheaply than by designing new substrate integrated circuitry. Multichip module technology is advantageous because of the density increase. With increased density comes equivalent improvements in signal propagation speed and overall device weight unmatched by other means. Current multichip module construction typically consists of a

printed circuit board substrate to which a series of integrated circuit components are directly adhered.

Many semiconductor chip fabrication methods package individual dies in a protecting, encapsulating material. Electrical connections are made by wire bond or tape to external pin leads adapted for plugging into sockets on a circuit board. However, with multichip module constructions, non-encapsulated chips or dies are secured to a substrate, typically using adhesive, and have outwardly exposed bonding pads. Wire or other bonding is then made between the bonding pads on the unpackaged chips and electrical leads on the substrate.

Much of the integrity/reliability testing of multichip module dies is not conducted until the chip is substantially complete in its construction. Considerable reliability testing must be conducted prior to shipment. In one aspect, existing technology provides temporary wire bonds to the wire pads on the die for performing the various required tests. However, this is a low-volume operation and further requires the test bond wire to ultimately be removed. This can lead to irreparable damage, thus effectively destroying the chip.

Another prior art test technique uses a series of pointed probes which are aligned to physically engage the various bonding pads on a chip. One probe is provided for engaging each bonding pad for providing a desired electrical connection. One drawback with such testing is that the pins undesirably on occasion penetrate completely

through the bonding pads, or scratch the bonding pads possibly leading to chip ruin.

It would be desirable to overcome these and other drawbacks associated with testing semiconductor circuitry for operability.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic representation of a fragment of a substrate processed in accordance with the invention.

Fig. 2 is a view of the Fig. 1 substrate fragment at a processing step subsequent to that shown by Fig. 1.

Fig. 3 is a perspective view of the Fig. 2 substrate fragment.

Fig. 4 is a view of the Fig. 1 substrate fragment at a processing step subsequent to that shown by Fig. 2.

Fig. 5 is a view of the Fig. 1 substrate fragment at a processing step subsequent to that shown by Fig. 4.

Fig. 6 is a perspective view of the Fig. 5 substrate fragment.

Fig. 7 is a view of the Fig. 1 substrate fragment at a processing step subsequent to that shown by Fig. 5.

Fig. 8 is a view of the Fig. 1 substrate fragment at a processing step subsequent to that shown by Fig. 7.

Fig. 9 is a perspective view of a substrate fragment processed in accordance with the invention.

Fig. 10 is a view of a substrate fragment processed in accordance with the invention.

Fig. 11 is a view of the Fig. 10 substrate fragment at a processing step subsequent to that shown by Fig. 10.

Fig. 12 is a view of the Fig. 10 substrate fragment at a processing step subsequent to that shown by Fig. 11.

Fig. 13 is a view of the Fig. 10 substrate fragment at a processing step subsequent to that shown by Fig. 12.

Fig. 14 is a view of the Fig. 13 substrate in a testing method in accordance with the invention.

Fig. 15 is a view of a substrate fragment processed in accordance with the invention.

Fig. 16 is a view of the Fig. 15 substrate fragment at a processing step subsequent to that shown by Fig. 15.

Fig. 17 is a view of the Fig. 15 substrate fragment at a processing step subsequent to that shown by Fig. 16.

Fig. 18 is a view of a substrate fragment processed ia accordance with the invention.

Fig. 19 is a view of the Fig. 18 substrate fragment at a processing step subsequent to that shown by Fig. 18.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

In accordance with one aspect of the invention, a method of engaging electrically conductive test pads on a semiconductor substrate having integrated circuitry for operability testing thereof comprises the following sequential steps:

providing an engagement probe having an outer surface comprising a grouping of a plurality of electrically conductive projecting apexes positioned in proximity to one another to engage a single test pad on a semiconductor substrate;

engaging the grouping of apexes with the single test pad on the semiconductor substrate; and

sending an electric signal between the grouping of apexes and test pad to evaluate operability of integrated circuitry on the semiconductor substrate.

In accordance with another aspect of the invention, a method of forming a testing apparatus for engaging electrically conductive test pads on a semiconductor substrate having integrated circuitry for operability testing thereof, comprises the following steps:

providing a locally substantially planar outer surface of a first material on a semiconductor substrate;

providing a layer of second material atop the substantially planar outer surface of first material, the second material being capable of substantially masking the underlying first material;

patterning and etching the layer of second material to selectively outwardly expose the first material and define a grouping of discrete first material masking blocks, the discrete first material masking blocks of the grouping having respective centers, the respective centers of the grouping being positioned in sufficient proximity to one another such that the centers of the grouping fall within confines of a given single test pad which the apparatus is adapted to electrically engage;

forming projecting apexes beneath the masking blocks at the masking block centers, the projecting apexes forming a group falling within the confines of the given single test pad of which the apparatus is adapted to electrically engage;

removing the discrete first material masking blocks from the substrate after the exposing step; and

rendering the projecting apexes electrically conductive.

In accordance with yet another aspect of the invention, a testing apparatus for engaging electrically conductive test pads on a semiconductor substrate having integrated circuitry for operability testing thereof comprises:

a test substrate; and

an engagement probe projecting from the test substrate to engage a single test pad on a semiconductor substrate having integrated

circuitry formed in the semiconductor substrate, the engagement probe having an outer surface comprising a grouping of a plurality of electrically conductive projecting apexes positioned in sufficient proximity to one another to collectively engage the single test pad.

The discussion proceeds initially with description of methods for forming testing apparatus in accordance with the invention, and to testing apparatus construction. Fig. 1 illustrates a semiconductor substrate fragment 10 comprised of a bulk substrate 12, preferably constituting monocrystalline silicon. Substrate 12 includes a locally substantially planar outer surface 14 comprised of a first material. In a preferred and the described embodiment, the first material constitutes the material of bulk substrate 12, and is accordingly silicon. A layer 16 of second material is provided atop the planar outer surface 14 of the first material. The composition of the second material is selected to be capable of substantially masking the underlying first material from oxidation when the semiconductor substrate is exposed to oxidizing conditions. Where the underlying first material comprises silicon, an example and preferred second material is Si_3N_4. A typical thickness for layer 16 would be from about 500 Angstroms to about 3000 Angstroms, with about 1600 Angstroms being preferred.

Referring to Figs. 2 and 3, second material layer 16 is patterned and etched to selectively outwardly expose the first material and define a grouping of discrete first material masking blocks 18, 20, 24 and 26. For purposes of the continuing discussion, the discrete first material

masking blocks of the grouping have respective centers. The lead lines in Fig. 2 depicting each of blocks 18, 20, 22 and 24 point directly to the lateral centers of the respective blocks. The respective centers of the grouping are positioned in sufficient proximity to one another such that the centers of the grouping will fall within the confines of a given single test pad of which the apparatus is ultimately adapted to electrically engage for test. Such will become more apparent from the continuing discussion.

As evidenced from Fig. 3, masking blocks 18, 20, 24 and 26 are patterned in the form of lines or runners integrally joined with other masking blocks/lines 28, 30, 32 and 34. The blocks/lines interconnect as shown to form first and second polygons 36, 38, with polygon 38 being received entirely within polygon 36. Polygons 36 and 38 constitute a grouping 41 masking blocks the confines of which fall within the area of a given single test pad of which the apparatus is ultimately adapted to electrically engage for test.

Referring to Fig. 4, semiconductor substrate 10 is exposed to oxidizing conditions effective to oxidize the exposed outer surfaces of first material. Such oxidizes a sufficient quantity of first material in a somewhat isotropic manner to form projecting apexes 40, 42, 44 and 46 forming a group 43 which, as a result of the patterning of the preferred nitride layer 16, fall within the confines of the given single test pad of which the apparatus is adapted to electrically engage. Such produces the illustrated oxidized layer 48. Example oxidizing conditions

to produce such effect would be a wet oxidation, whereby oxygen is bubbled through H_2O while the substrate is exposed to 950°C.

Referring to Fig. 5, the oxidized first material 48 is stripped from the substrate. Example conditions for conducting such stripping would include a hot H_3PO_4 wet etch. Thereafter, the discrete first material masking blocks 18, 20, 24, 26, 28, 30, 32 and 34 are removed from the substrate. An example condition for such stripping in a manner which is selective to the underlying silicon apexes include a room temperature HF wet etch. Thus referring to Fig. 6, the steps of patterning and etching, exposing, and stripping form projecting apexes beneath the masking blocks at the masking block centers, such projecting apexes being numbered 40, 42, 44, 46, 48, 50, 52 and 54, which are in the form of multiple knife-edge lines. The knife-edge lines interconnect to form the illustrated polygons 36 and 38. The apexes and correspondingly knife-edged or pyramid formed polygons are sized and positioned in sufficient proximity to fall within the confines of a single test pad of which the apparatus is adapted to engage, as will be more apparent from the continuing discussion.

Other ways could be utilized to form projecting apexes beneath the masking blocks at the masking block centers. As but one example, a wet or dry isotropic etch in place of the step depicted by Fig. 4 could be utilized. Such etching provides the effect of undercutting more material from directly beneath the masking blocks to create apexes, as such areas or regions have greater time exposure to etching.

Referring again to Fig. 5, the oxidation step produces the illustrated apexes which project from a common plane 56. For purposes of the continuing discussion, the apexes can be considered as having respective tips 58 and bases 60, with bases 60 being coincident with common plane 56. For clarity, tip and base pairs are numbered only with reference to apexes 40 and 42. Bases 60 of adjacent projecting apexes are spaced from one another a distance sufficient to define a penetration stop plane 62 therebetween. Example spacings between apexes would be 1 micron, while an example length of an individual stop plane would be from 3 to 10 microns. The function of penetration stop plane 62 will be apparent from the continuing discussion. A tip 58 and base 60 are provided at a projecting distance apart which is preferably designed to be about one-half the thickness of the test pad which the given apparatus is adapted to engage.

Multiple oxidizing and stripping steps might be conducted to further sharpen and shrink the illustrated projecting apexes. For example and again with reference to Fig. 4, the illustrated construction in such multiple steps would have layer 48 stripped leaving the illustrated masking blocks in place over the apexes. Then, the substrate would be subjected to another oxidation step which would further oxidize substrate first material 12, both downwardly and somewhat laterally in the direction of the apexes, thus likely further sharpening the apexes. Then, the subsequently oxidized layer would be stripped

from the substrate, thus resulting in deeper, sharper projections relative from a projecting plane.

Referring to Fig. 7, apex group 43 is covered a nitride masking layer 64 and photopatterned. Referring to Fig. 8, silicon substrate 12 is then etched into around the masked projecting apexes to form a projection 64 outwardly of which grouping 43 of the projecting apexes project. The masking material is then stripped.

More typically, multiple groups of projecting apexes and projections would be provided, with each being adapted to engage a given test pad on a particular chip. Further tiering for producing electrically contact-engaging probes might also be conducted. Fig. 9 illustrates such a construction having apex groups 43a and 43b formed atop respect projection 64a and 64b. A typical projecting distance from base 60 to tip 58 would be 0.5 microns, with a projection 64 being 100 microns deep and 50 microns wide. Projections 64a and 64b in turn have been formed atop elongated projections 66a and 66b, respectively. Such provides effective projecting platforms for engaging test pads as will be apparent from the continuing discussion.

Next, the group of projecting apexes is rendered electrically conductive, and connected with appropriate circuitry for providing a testing function. The discussion proceeds with reference to Figs. 10-13 for a first example method for doing so. Referring first to Fig. 10, a substrate includes a pair of projections 64c and 64d having respective outwardly projecting apex groups 43c and 43d. A layer of photoresist

is deposited atop the substrate and patterned to provide photoresist blocks 68 as shown. Photoresist applies atop a substrate as a liquid, thus filling valleys in a substrate initially and not coating outermost projections. Thus, the providing of photoresist to form blocks 68 is conducted to outwardly exposed projecting apex groups 43c and 43d, as well as selected area 70 adjacent thereto. Photoresist blocks 68 covers selected remaining portions of the underlying substrate.

Referring to Fig. 11, electric current is applied to substrate 12 to be effective to electroplate a layer of metal 72 onto outwardly exposed projecting apex groupings 43c and 43d and adjacent area 70. An example material for layer 72 would be electroplated Ni, Al, Cu, etc. An example voltage and current where substrate 12 comprises silicon would be 100V and 1 milliamp, respectively. Under such conditions, photoresist functions as an effective insulator such that metal deposition only occurs on the electrically active surfaces in accordance with electroplating techniques. Photoresist is then stripped from the substrate, leaving the Fig. 11 illustrated construction shown, which may also include a desired conductive runner 74 formed atop bulk substrate 12 between projections 64c and 64d.

The preferred material for metal layer 72 is platinum, due to its excellent oxidation resistance. Unfortunately, it is difficult to directly bond the typical copper or gold bonding wires to platinum. Accordingly, preferably an intervening aluminum bonding site is provided. Referring to Fig. 12, an aluminum or aluminum alloy layer 76 is

blanket deposited atop the substrate. A layer of photoresist is deposited and patterned to provide photoresist masking blocks 78. The substrate would then be subjected to an etch of the aluminum material in a manner which was selective to the underlying platinum. Example etching conditions would include a hot H_3PO_4 wet etch. Such leaves resulting elevated bonding blocks 80 of aluminum atop which a bonding wire 82 is conventionally bonded, as shown in Fig. 13.

The description proceeds with reference to Fig. 14 for utilizing such an apparatus for conducting electrical tests of a chip. Fig. 14 illustrates the testing apparatus of Fig. 13 engaging a chip 85 which is being tested. Chip 85 comprises a substrate portion 86 and outwardly exposed bonding pads 88. Protecting or encapsulating material 90 is provided such that substrate 86 and circuitry associated therewith is protected, with only bonding pads 88 being outwardly exposed. Bonding pads 88 have some thickness "A".

Substrate 12 comprises a test substrate having engagement probes 64c and 64d projecting therefrom. Such include respective electrically conductive apexes groups 43c and 43d positioned in respective proximity to fall within the confines of and engage a single test pad 88 on chip 85. Such apexes are engaged with the respective test pads, as shown.

The illustrated projecting apexes actually project in to half-way into the thickness of the bonding pads, a distance of approximately on-half "A". The penetration stop surface 62 described with reference

to Fig. 5 provides a stopping point for preventing the projecting points from extending further into bonding pads 88 than would be desired. In connecting the testing apparatus to chip 85, pressure would be monitored during engagement of the projecting tips relative to the pads 88. At some point during the projection, the force or back pressure against the testing apparatus would geometrically increase as the penetration stop plane reaches the outer surface of the bonding pads 88, indicating that full penetration had occurred. At this point, the testing substrate and chip 85 would be effectively electrically engaged. An electric signal would be sent between the respective grouping of apexes and respective test pads in conventional testing methods to evaluate operability of integrated circuitry formed within the semiconductor substrate 85.

Reference is made to Figs. 15-17 for a description of an alternate method of rendering projecting apexes electrically conductive.

Starting with Fig. 15, such are sectional views taken laterally through projection 64a of Fig. 9. Referring to Fig. 16, an electrically conductive nucleation layer 90 is blanket deposited atop the apexes and substrate. An example material would be elemental nickel deposited by sputter techniques. Photoresist is then applied and patterned as shown to produce photoresist blocks 92. Thus, the nucleation layer coated projecting apexes and selected area adjacent thereto is outwardly exposed, while selected remaining nucleation layer coated portions of the substrate are coated by resist blocks 92. At this point, a current is

applied to nucleation layer 90 effective to electrodeposit a layer 94, such as electroless deposited copper, to a thickness of 1 micron. Resist blocks 92 effectively insulate underlying nucleation layer 90 from depositing copper atop the resist. An example voltage and current would be 5V and 1 milliamp, respectively.

Referring to Fig. 17, the resist is then stripped from the substrate. A dry plasma etch is then conducted which selectively removes the exposed nickel nucleation layer 90 relative to copper layer 94, such that only copper over the illustrated nickel remains. Then if desired and as shown, current is applied to the nucleation layer and copper material in a manner and under conditions which electroless deposits a 2000 Angstrom thick layer 96 of, for example, platinum, palladium or iridium. Wire bonding could then be conducted apart from apexes 43a utilizing an intervening block of aluminum.

Such technique is preferable to the previously described electroless deposition method in that lower voltage and current can be utilized in the electroless deposition method where a highly conductive nucleation layer is provided atop the substrate.

Another alternate and preferred technique for forming and rendering the projecting apexes conductive is shown with reference to Figs. 18 and 19. Such is an alternate construction corresponding to that construction shown by Fig. 10. Fig. 18 is the same as Fig. 10, but for the addition of, a) an insulating layer 71, preferably SiO_2; and b) a metal nucleation layer 73, prior to the providing and patterning

to produce photoresist blocks 68. Such a process is preferable to that shown by Fig. 10 to provide separation of the typical monocrystalline silicon substrate 12 from direct contact with metal. Fig. 19 illustrates the subsequent preferred electroless deposition of a metal layer 72 using substrate nucleation layer 73 as a voltage source. With respect to the embodiment shown by Figs. 15 - 17, such also would preferably be provided with an insulating layer prior to deposition of the nucleation layer. An alternate and preferred material for layer 73 would be aluminum metal, with the subsequently electroless layer being comprised essentially of platinum. Platinum could then be used as a masking layer to etch exposed aluminum after photoresist strip. An example etch chemistry for such etch would include a wet H_3PO_4 dip.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.